Please type a plus sign (+) inside this box → [+]

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Patent and Trademark Office. U.S. DEPARTMENT OF COMMERCE

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1 53(b))

Attorney Docket No.	41367-2000300	Total Pages	*
First Named Inventor or Application Identifier			
Olson, Erlend			
Express Mail Label No.	EJ499951597US		

CERTIFICATE OF MAILING BY "EXPRESS MAIL"

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Barbara L. Phillips

Barbara L. Phillips

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] Fee Transmittal Form
(Submit an original, and a duplicate for fee processing)
2. [X] Specification [Total Pages 12*]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R & D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claim(s)
- Abstract of the Disclosure
3. *[X] Drawing(s) (35 USC 113) [Total Sheets *11]
4. *[X] Oath or Declaration [Total Pages *3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d)
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b)
5. [ ] Incorporation By Reference (useable if Box 4b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein

6.* [ ] Microfiche Computer Program (Appendix)

7.* Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8.* [ ] Assignment Papers (cover sheet & document(s))
9.* [ ] 37 CFR 3.73(b) Statement (when there is an assignee) [X] Power of Attorney (Unsigned)
10.* [ ] English Translation Document (if applicable)
11.* [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12.* [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14.* [X] Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15.* [ ] Certified Copy of Priority Document(s) (if foreign priority is claimed)
16.* [ ] ....

17. If a CONTINUING APPLICATION, check appropriate box and supply the requisite information:

*[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: *

18. CORRESPONDENCE ADDRESS

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☒ If a paper is untimely filed in the above-referenced application by applicant or his/her representative, the Assistant Commissioner is hereby petitioned under 37 C.F.R. § 1.136(a) for the minimum extension of time required to make said paper timely. In the event a petition for extension of time is made under the provisions of this paragraph, the Assistant Commissioner is hereby requested to charge any fee required under 37 C.F.R. § 1.17(a)-(d) to **Deposit Account No. 03-1952.** However, the Assistant Commissioner is **NOT** authorized to charge the cost of the issue fee to the Deposit Account.

The filing fee has been calculated as follows:

FOR	NUMBER FILED	NUMBER EXTRA	RATE	CALCULATIONS
TOTAL CLAIMS	* - 20 =	*	x $18.00	$*
INDEPENDENT CLAIMS	* - 3 =	*	x $78.00	$*
MULTIPLE DEPENDENT CLAIM(S) (if applicable)			+ $260.00	$*
			BASIC FEE	$760.00
		TOTAL OF ABOVE CALCULATIONS =		$760.00
Reduction by 1/2 for filing by small entity (Note 37 C.F.R. §§ 1.9, 1.27, 1.28). If applicable, verified statement must be attached.				$380.00
Assignment Recording Fee (if enclosed)				
			TOTAL =	$380.00

☒ A check in the amount of $380.00 is attached.

☐ Charge $380.00 to **Deposit Account No. 03-1952** referencing docket no. 41367-2000300.

Applicants hereby petition for any required relief, including extensions of time, and authorize the Assistant Commissioner to charge the cost of such petitions and/or other fees or to credit any overpayment to **Deposit Account No. 03-1952** referencing docket no. 41367-2000300. A duplicate copy of this transmittal is enclosed, for that purpose.

Dated: June 30, 1999

Respectfully submitted,

By: Jimmy M. Shin

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Applicant/Patentee: Olson, Erlend; Opris, Ion
Serial No./Patent No.: *
Filed on/Issued: *
Docket No.: PTC30001.00
Client Reference: *
For: METHOD AND APPARATUS FOR EFFICIENT MIXED SIGNAL PROCESSING IN A DIGITAL AMPLIFIER

VERIFIED STATEMENT CLAIMING SMALL ENTITY STATUS
37 C.F.R. §§ 1.9(f) AND 1.27(c) — SMALL BUSINESS CONCERN

I hereby declare that I am

- ☐ the owner of the small business concern identified below.
- ☒ an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN: Pivotal Technologies Corporation

ADDRESS OF CONCERN: 70 S. LAKE Suite 900 Pasadena CA 91101

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 C.F.R. § 121.12, and reproduced in 37 C.F.R. § 1.9(d), for purposes of paying reduced fees to the United States Patent and Trademark Office, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled METHOD AND APPARATUS FOR EFFICIENT MIXED SIGNAL PROCESSING IN A DIGITAL AMPLIFIER by inventors Erlend Olson and Ion Opris described in

- ☒ the specification filed herewith with title as listed above.
- ☐ the application identified above.
- ☐ the patent identified above.

If the rights held by the above identified business concern are not exclusive, each individual, concern or organization having rights in the invention must file separate verified statements averring to their status as small entities, and no rights to the invention are held by any person, other than the inventor, who would not qualify as an independent inventor under 37 C.F.R. § 1.9(c) if that person made the invention, or by any concern which would not qualify as a small business concern under 37 C.F.R. § 1.9(d), or a nonprofit organization under 37 C.F.R. § 1.9(e).

Each person, concern or organization having any rights in the invention is listed below:

- ☒ no such person, concern, or organization exists.
- ☐ each such person, concern or organization is listed below.

NAME	ADDRESS	TYPE
		☐ Individual ☐ Small Business Concern ☐ Nonprofit Organization

Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 C.F.R. § 1.27)

I acknowledge the duty to file, in this application or patent, notification or any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 C.F.R. § 1.28(b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING: * Erlend Olson
TITLE OF PERSON IF OTHER THAN OWNER: * Chief Tech Officer
ADDRESS OF PERSON SIGNING: * 70 S. LAKE Suite 900 Pasadena CA 91101

SIGNATURE: [signature] DATE: 6-30-99

PTO/SB/10 (10-92)
la-305165

METHOD AND APPARATUS FOR EFFICIENT MIXED SIGNAL PROCESSING IN A DIGITAL AMPLIFIER

Inventors: E. Olson
I. Opris

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to the field of switching amplifiers. More specifically, the present invention relates to a novel method of sampling in the signal modulation stage of a digital amplifier to achieve a highly accurate representation of the input signal at substantial gain.

2. Description of the Related Art

There have been various developments pertaining to oversampled, noise-shaping signal processing. These developments have been applicable to both continuous-time (analog) and discrete-time (digital or sampled analog) signals. The constant struggle in this field is to increase the efficiency of the amplifiers. Given the myriad of applications of sound applications in the electronics of today, it is apparent that an efficient audio amplification is highly desirable.

In response to this need, attempts have been made to design switching audio amplifiers using oversampled, noise-shaping modulators, especially delta-sigma modulators. A prior art first order delta-sigma modulator is shown in FIG. 1. A noise shaping network 102 is connected in series with a comparator 104, which is a 1-bit quantizer with sampling rate f_s. The output 105 of the comparator is fed back to the noise shaping network via summation element 106. The feedback in turn forces the

average value of the quantized output signal to track the average value of the input to the modulator 100. Any difference between the quantized output and modulator input is accumulated in the noise shaping network 102 and eventually corrected. For first-order delta-sigma modulators, noise in the signal band due to quantization error is reduced by approximately 9 dB for each doubling of the oversampling ratio (OSR). The OSR is given by $f_s/2f_o$, where $2f_o$ is the Nyquist rate, i.e., twice the bandwidth f_o of the baseband signal, and f_s is the previously mentioned 1-bit quantizer's sampling rate. For second-order delta-sigma modulators, this noise is reduced by approximately 15 dB (9 dB + 6 dB) for the same increase in OSR. However, noise improvements achieved by increases in the OSR, i.e., increases in f_s, are ultimately limited as the rise and fall times of the output signal become significant with respect to the sample period.

Accordingly, it would be highly desirable to employ aggressive noise shaping while at the same time maintaining a fixed signal feedback rate for improved noise shaping. This would allow efficient application of audio amplification in many of today's electronics such as multimedia computers.

SUMMARY OF THE INVENTION

A system and method of creating a highly efficient digital amplifier which can take either analog or digital inputs, and produce a high power accurate representation of the input to drive speakers or other low impedance load is described. The system employs a transition detector and delay unit which allows the comparator of the signal modulator to ignore its inputs for a pre-determined number of subsequent clock cycles once an output transition has been detected. Through the use of faster clocks and variable clock cycle skips upon the comparator's output transition, finer resolution of the feedback's clock period for noise-shaping purposes is achieved. Finer resolution of the clock period allows the present invention to employ a more aggressive noise-shaping than previously possible.

In another aspect of the invention, additional delta-sigma modulator noise suppression is obtained by using the common bridge implementation of the power output stage with the improvement of configuring the bridge to create a 3-state condition instead of the conventional 2 states. By controlling the two halves of the bridge independently of one another, an output with 3 states makes for improved noise shaping performance.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a schematic representation of a prior art first order delta-sigma modulator;

Figure 2A is a schematic representation of one embodiment of a digital amplifier which incorporates the present invention for processing digital inputs;

Figure 2B is a schematic representation of one embodiment of a digital amplifier that incorporates the present invention for processing analog inputs;

Figure 3 is a schematic representation of the new implementation of a sigma-delta modulator in accordance with the present invention;

Figure 4 is a schematic representation of an embodiment of the transition detector and delay unit of Figure 3;

Figure 5 is a schematic representation of a single-loop 1-bit feedback 6th order sigma-delta modulator which incorporates the present invention;

Figure 6 is a graph of the signal spectrum for a conventional 6th order delta-sigma modulator with F_{clock} = 1 MHz;

Figure 7 is a graph of the signal spectrum for a 6th order delta-sigma modulator with F_{clock} = 10 MHz and N=10 according to an embodiment of the present invention;

Figure 8 is a schematic representation of bridge output as existing in the prior art;

Figure 9 is a schematic representation of bridge circuit in accordance with one embodiment of the present invention; and

Figure 10 is an output diagram of the bridge circuit in Figure 9.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

The present description is of the best presently contemplated mode of carrying out the invention. This description is made for the purpose of illustrating the general principles of the invention and should not to be taken in a limiting sense. The scope of the invention is best determined by reference to the appended claims.

The present invention will be described in reference to a 1-bit digital amplifier 200. Referring to FIG. 2A, the input may be a digital signal 202 consisting of typically a 16 bit or 18 bit digital input. In this example, it may be a digital audio input at 48 kHz. A digital interpolation filter 204, converts the low rate, multi-bit signal 202 to a high rate multi-bit signal 206. The signal 206 consists of typically 16 to 22 bits in an audio application at a sample rate of typically 32 to 128 times the original sample rate at 202. An additional digital filter 208 can also be added, which performs two functions. First, it performs a typical crossover function commonly used in audio to divide up the frequency content of the incoming signal 202, in order to more carefully parameterize for proper reproduction of signals through the subsequent signal path. Second, it performs a pre-warping of the signal frequency content such that after the signal 210 is subsequently warped through the non-linear mechanical response of the speaker 218, the resulting audio has flat frequency response to the listener. The signal 210 then enters the new type of delta-sigma modulator 212. This new type of modulator, further described below, then outputs a signal 214 which possess certain special characteristics also further described below. Finally, the signal at 214 then drive a typical H-bridge controller 216, which directly drives the speakers 218.

Referring to Fig 2B, the core of the 1-bit digital amplifier, consisting of the delta-sigma modulator 212 and the H bridge controller 216, can also be used in an

embodiment that receives an analog signal 203, instead of a digital signal 202. For the analog input signal 203, an interpolation filter is not required.

Referring to FIG. 3, delta-sigma modulator 212 of FIG. 2 is shown in further detail. The configuration may be applied to any single loop 1-bit feedback delta-sigma modulator as indicated in FIG. 1. In FIG. 3, output 214 of the comparator 104 is fed back to the noise shaping network along with input 210 via summation element 106. The noise shaping network 102 is coupled to the comparator 104 which is then coupled to the transition detector and delay unit 308. The output 310 of the transition detector and delay unit 308 provides the inputs of the AND gate 316. The output 318 of the AND gate 316 provides the clock input of the comparator 104. This clock input 318 determines the moment when the comparator output 214 gets updated. The transition detector and delay unit 308 allows the comparator 104 to ignore its inputs for a pre-determined number of subsequent clock cycles once an output transition has been detected. In other words, when the comparator output 214 goes through a transition (e.g., from 0 to 1 or from 1 to 0), the output 310 from the transition detector and delay unit 308 is always a "0" to disable the comparator 104. The comparator 104 in such an instance is disabled since the output 318 of the AND gate 316 will always be a "0" if at least one of its inputs is a "0". A possible implementation of the of the transition detector and delay unit 308 is shown in FIG. 4. In this implementation, N flip-flops 410, 412, and so forth are employed to provide an output 310 such that inputs to the comparator 104 will be ignored for a period of N clock cycles following a transition in the comparator output 214. Thus, N is a variable value which may be adjusted to achieve specified results. As illustrated in FIG. 4, the transition detector and delay unit 308 employs a NOR gate 402 and an AND gate 404. Basically, the OR gate 406 will provide output 450 of "1" if either output 430 from the NOR gate 402 or the output 440 from the AND gate 404 is a "1". The only way for a NOR gate to produce an output of "1" is to have all its inputs be

"0". The only way for an AND gate to produce an output of "1" is to have all its inputs be "1". Therefore, it is clear that any combination of "0" and "1" as the inputs for either the NOR gate 402 or AND gate 404 will result in each respective output to be "0". This configuration allows the comparator 104 to effectively ignore its inputs 210 for a pre-determined number of clock cycles once its output 214 has gone through a transition.

The end result of this arrangement is that the comparator output 214, and therefore the drive signal 214 for the H-bridge controller 216, cannot change states faster than the clock frequency of the delta-sigma modulator divided by N, which is significantly lower than the clock frequency. Since the feedback 214 in the 1-bit delta sigma modulator (FIG. 1) is basically disabled during the non-responsive period (N clock cycles) of the comparator 104, the stability of the loop is affected. Therefore, the noise shaping afforded by the delta-sigma converter has to be less aggressive than that typically cited in such designs where the feedback is expected to be responsive at the clock frequency. However, this is assuming that the clock frequency of the modulator remains the same. If a faster clock is employed to offset the increasing value of N, then the comparator response and hence the feedback signal is a feedback at the frequency of the faster clock divided by N, but with a finer resolution of the clock period, since the "high" or "low" output of the comparator can exist for N clocks, N+1 clocks, N+2 clocks, and so on.

For example, assume that for N=1, a clock with a frequency of 1 MHz (period of 1μs) is used in the modulator. So, with N=1, there is no delay caused by the transition in comparator output and the feedback occurs at a frequency of 1 MHz. Now, assume that for N=10, a clock with a frequency of 10 MHz (period of 1/10 μs) is used in the modulator. Then, every transition of the comparator output causes the comparator to ignore its inputs for 10 clock cycles. However, since the faster clock has a frequency of 10 MHz, the feedback frequency is still 1 MHz (10 MHz divided

by N=10). With the feedback frequency remaining the same by using a faster clock, this invention maintains the desired feedback frequency rate while at the same time achieving finer resolution of the clock period of 1/10 μs. Finer resolution of the clock period allows the present invention to employ a more aggressive noise-shaping than previously possible. A complete theory of delta-sigma modulator basic design can be found in "Delta -Sigma Data Converters - Theory, Design and Simulation" edited by S.R. Norsworthy, R. Schreier and G. Temes, IEEE Press, 1996 pp. 152-155 and pp. 178-183.

A noise shaping function that maintains stability with the approach described herein can be obtained by adjusting the coefficients of a standard noise shaping function. Unfortunately, since sigma-delta converters are based on the non-linear function of the 1-bit quantizer (the comparator), there is no general linear stability theory currently in existence for loop orders higher than two, but the stability of the loop can only be verified through simulations.

A digital amplifier involving a conventional single-loop 1-bit feedback 6th order delta-sigma modulator 500 is shown in FIG. 5. Referring to FIG. 5, there are six summation elements 502, 504, 506, 508, 510, 512 coupled in series to six integrators 520, 522, 524, 526, 528, 530. The input 210 is fed into the system via summation element 502 and is eventually fed as the input to the comparator 104. The output 214 of the comparator 104 is fed back to each of the six summation elements of the modulator 500. An example of the output of such a digital amplifier with Fclock = 1 MHz which achieves 69 dB signal-to-noise ratio (SNR) in a 20 kHz BW, is shown in FIG. 6. It has an output clock, and hence comparator resolution and power device switching time of 1μs. By using a 10 MHz clock instead with N=10 (again then, the minimum comparator resolution is 1μs), in accordance with one embodiment of the present invention, the SNR in the same 20 kHz band is 90 dB, as

indicated by the signal-to-noise ratio (SNR) in FIG. 7. The feedback coefficients for this particular example are:

$a6 = 6(1-a)$

$a5 = 15(1-a)^2$

$a4 = 20(1-a)^3$

$a3 = 15(1-a)^4$

$a2 = 6(1-a)^5$

$a1 = (1-a)^6$

$g1 = 1.2E-4$

$g2 = 4.0E-5$

where a is a parameter close to 1 used for stability simulations (a=0.98 in this example), and g1 and g2 are resonator settings, as indicated in FIG. 5. As previously mentioned, the method is equally applicable to analog or digital implementations.

In another aspect of the invention, a novel technique employed in the H-bridge controller 216 of FIG. 2 is disclosed. It relates to the technique previously described for the delta-sigma converter. Referring to the prior art as shown in FIG. 8, the bridge Output P 810 and Output N 820 are dependent on one another. In other words, Output P 810 and Output N 820 are both $-V_{dd}$ or $+V_{dd}$. Thus, with the Output 830 = Output P 810 - Output N 820, the peak-to-peak maximum amplitude is $2V_{dd}$ (either $+2V_{dd}$ or $-2V_{dd}$). Additional delta-sigma modulator noise suppression can be obtained by using the common bridge implementation of the power output stage shown in FIG. 9, with the improvement of configuring the bridge to create a 3-state condition instead of the conventional 2 states. By controlling the two halves of the bridge independently of one another, Output P 910 and Output N 920 have values independent from one another. Thus, four different possible permutations exist for values of Output I 940 and Output II 950. The combination of these four values determine the three states of Output 930 value, since Output = Output I - Output II.

The Output 930 thus has three states as shown in FIG. 10. The delta-sigma modulator feedback can then also be interpreted as 3 states instead of only 2, and the noise-shaping performance of the loop is improved by an additional 3 dB. By adding the third state to the feedback the stability of the loop is improved and the noise shaping function can be designed more aggressively. Moreover, the gating mechanism for the two legs can be independent, so output changes faster than T_{clock}*N can occur at the output without any device in the H-bridge switching faster than F_{clock}/N. This result can be seen in FIG. 10, where the period of Output I and Output II at any given state (0 or 1) span at least as long as T_{clock}*N. However, because Output is equal to the value of Output I - Output II (a combination of two independent results), the period of Output's state (-1, 0, or 1) can be shorter than T_{clock}*N. Therefore, the state transition of Output may occur at a rate faster than F_{clock}/N.

Claims

What is claimed is:

1. A modulation stage for signal shaping comprising:

means for preliminary noise-shaping of an input signal; and

means for discrete-time sampling having a predetermined sampling frequency, the sampling means coupled to the noise-shaping means to produce an output signal with a lower transition rate with respect to said sampling frequency by a predetermined multiple.

2. A modulation stage for signal shaping of claim 1 wherein the means for discrete-time sampling further comprises means for suppressing sampling of the input signal for a set number of clock cycles.

3. A modulation stage for signal shaping of claim 2 wherein the means for suppressing comprises means for detecting a transition in the output signal.

4. A H-bridge controller wherein its outputs consist of three states.

5. A H-bridge controller of claim 4 wherein the gating mechanism for each leg is independently controlled.

6. A digital amplifier comprising:

a modulation stage for signal shaping; and

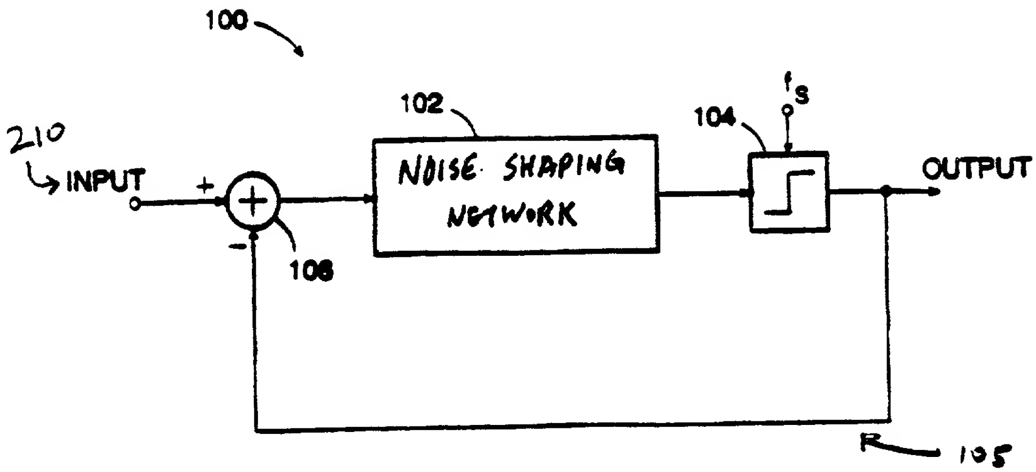
a H-bridge controller wherein its outputs consist of three states.

ABSTRACT OF THE DISCLOSURE

A system and method of creating a highly efficient digital amplifier which can take either analog or digital inputs, and produce a high power accurate representation of the input to drive speakers or other low impedance load is described. The system employs a transition detector and delay unit which allows the comparator of the signal modulator to ignore its inputs for a pre-determined number of subsequent clock cycles once an output transition has been detected. Through the use of faster clocks and variable clock cycle skips upon the comparator's output transition, finer resolution of the feedback's clock period for noise-shaping purposes is achieved. Finer resolution of the clock period allows the present invention to employ a more aggressive noise-shaping than previously possible.

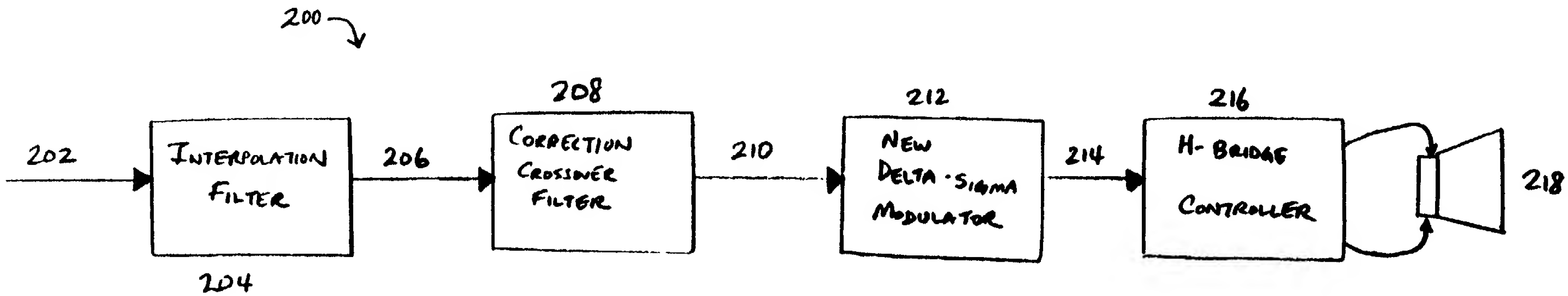
In another aspect of the invention, additional delta-sigma modulator noise suppression is obtained by using the common bridge implementation of the power output stage with the improvement of configuring the bridge to create a 3-state condition instead of the conventional 2 states. By controlling the two halves of the bridge independently of one another, an output with 3 states makes for improved noise shaping performance.

FIG. 1



PRIOR ART

FIG. 2A



200
202
Interpolation Filter
204
206
208
Correction Crossover Filter
210
212
New Delta-Sigma Modulator
214
216
H-Bridge Controller
218

FIG. 2B

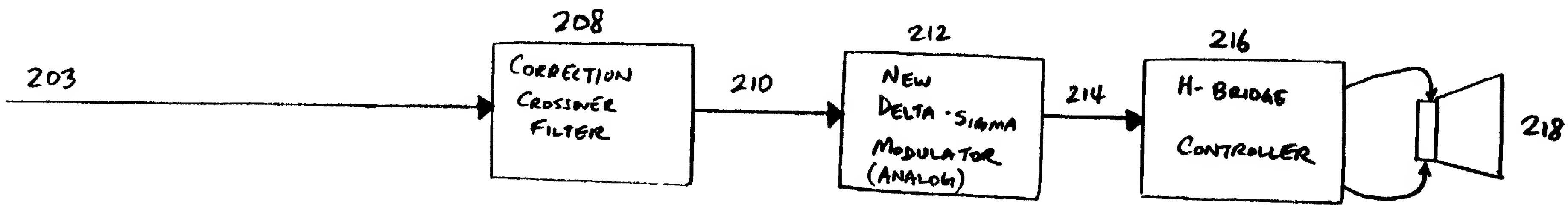
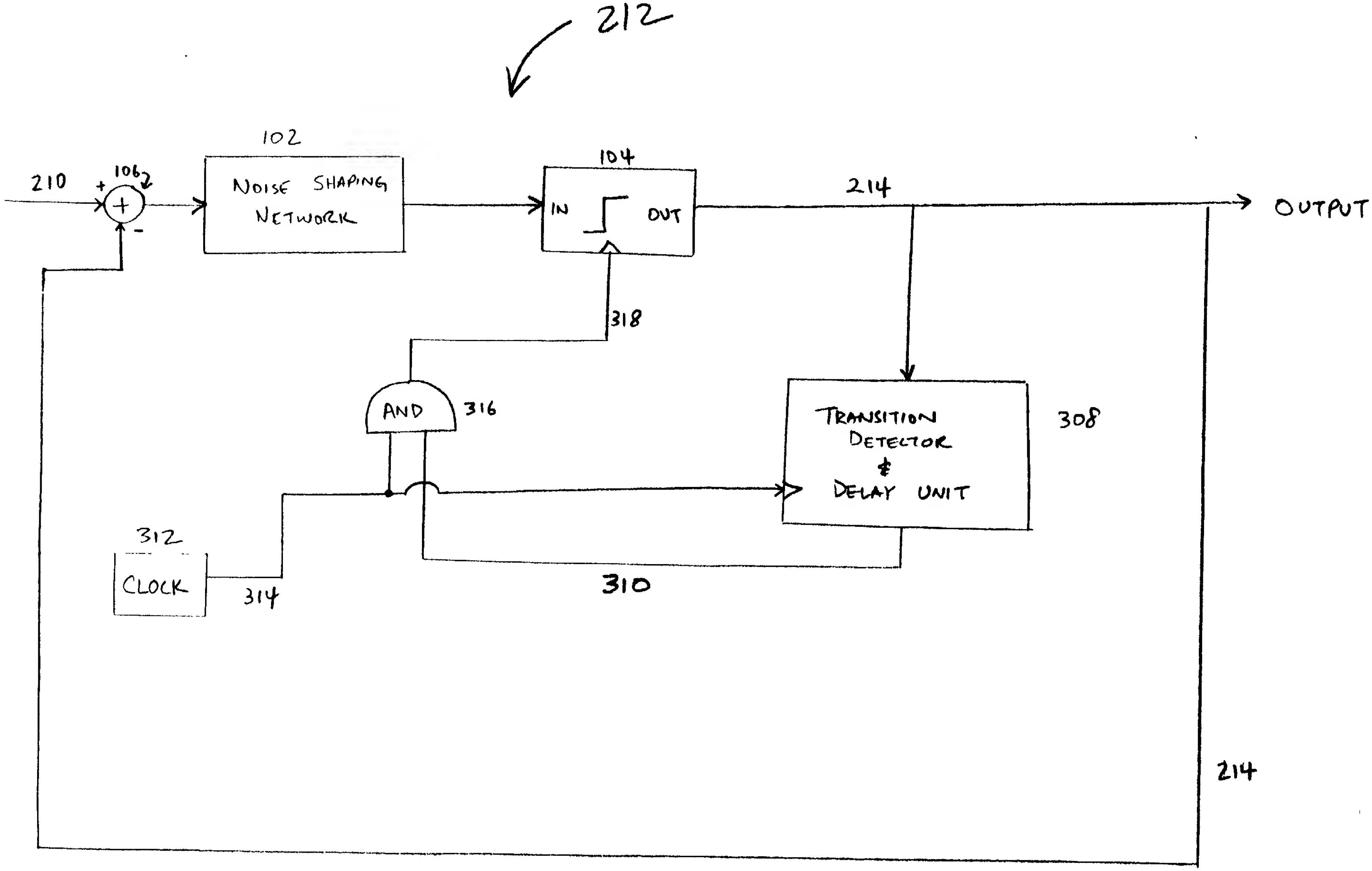

203
208
CORRECTION
CROSSOVER
FILTER
210
212
NEW
DELTA-SIGMA
MODULATOR
(ANALOG)
214
216
H-BRIDGE
CONTROLLER
218

FIG. 3



212
210
106
+
-
102
NOISE SHAPING NETWORK
104
IN
OUT
214
OUTPUT
318
AND
316
TRANSITION DETECTOR & DELAY UNIT
308
312
CLOCK
314
310
214

FIG 4

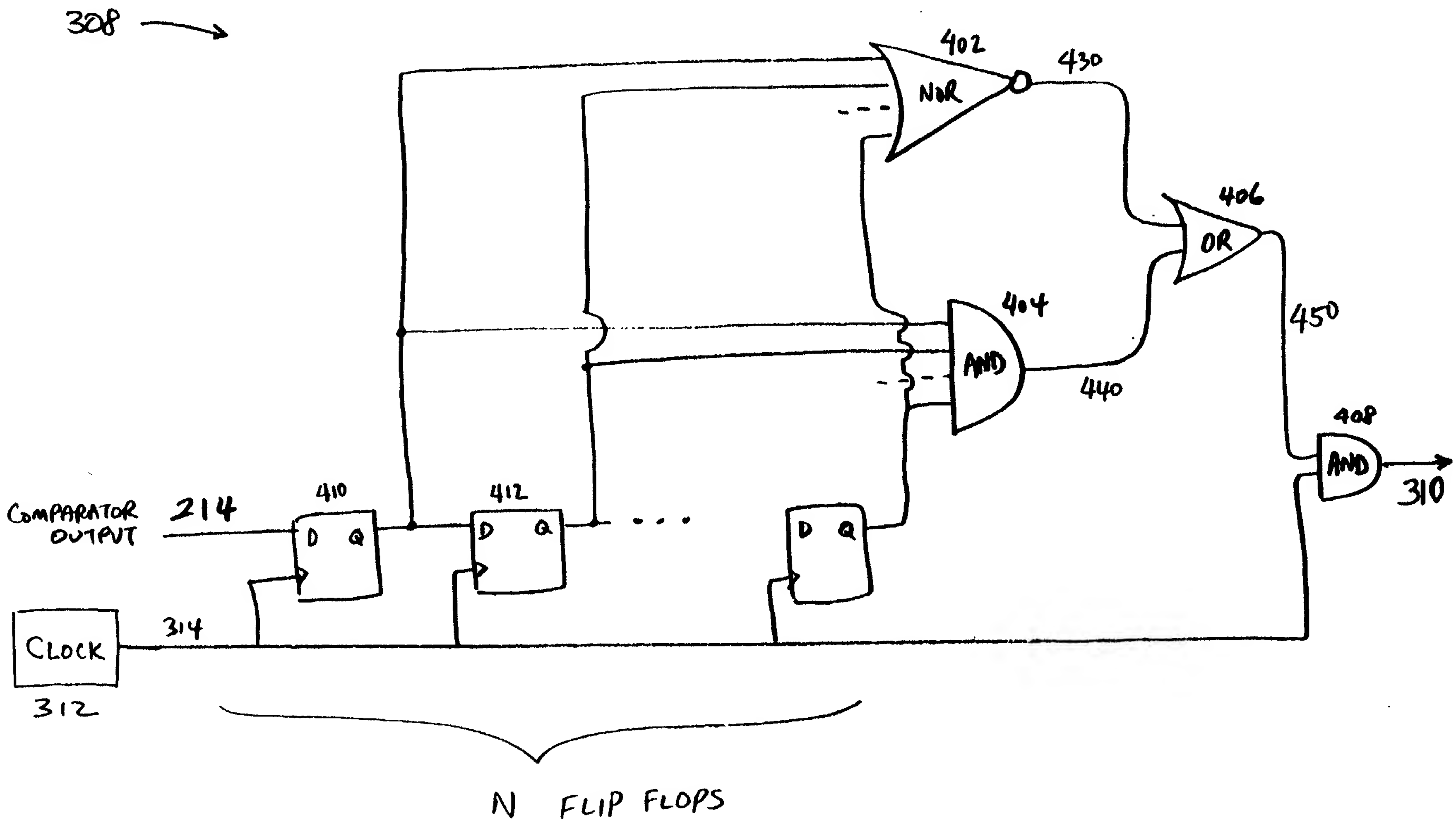
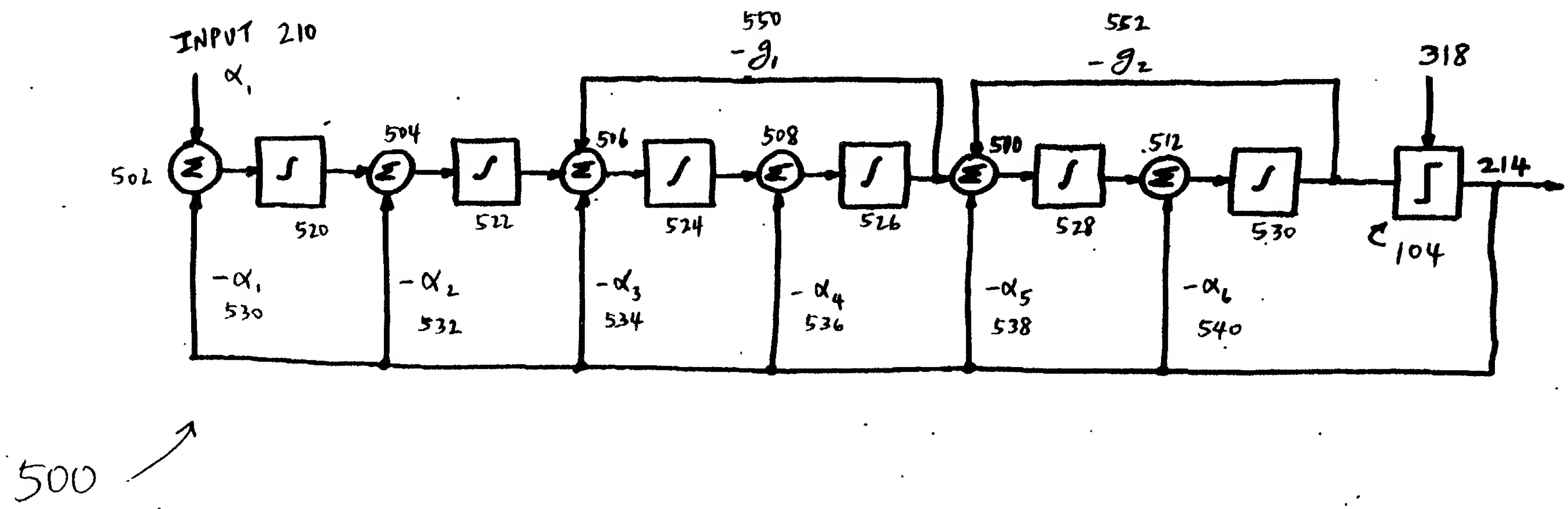
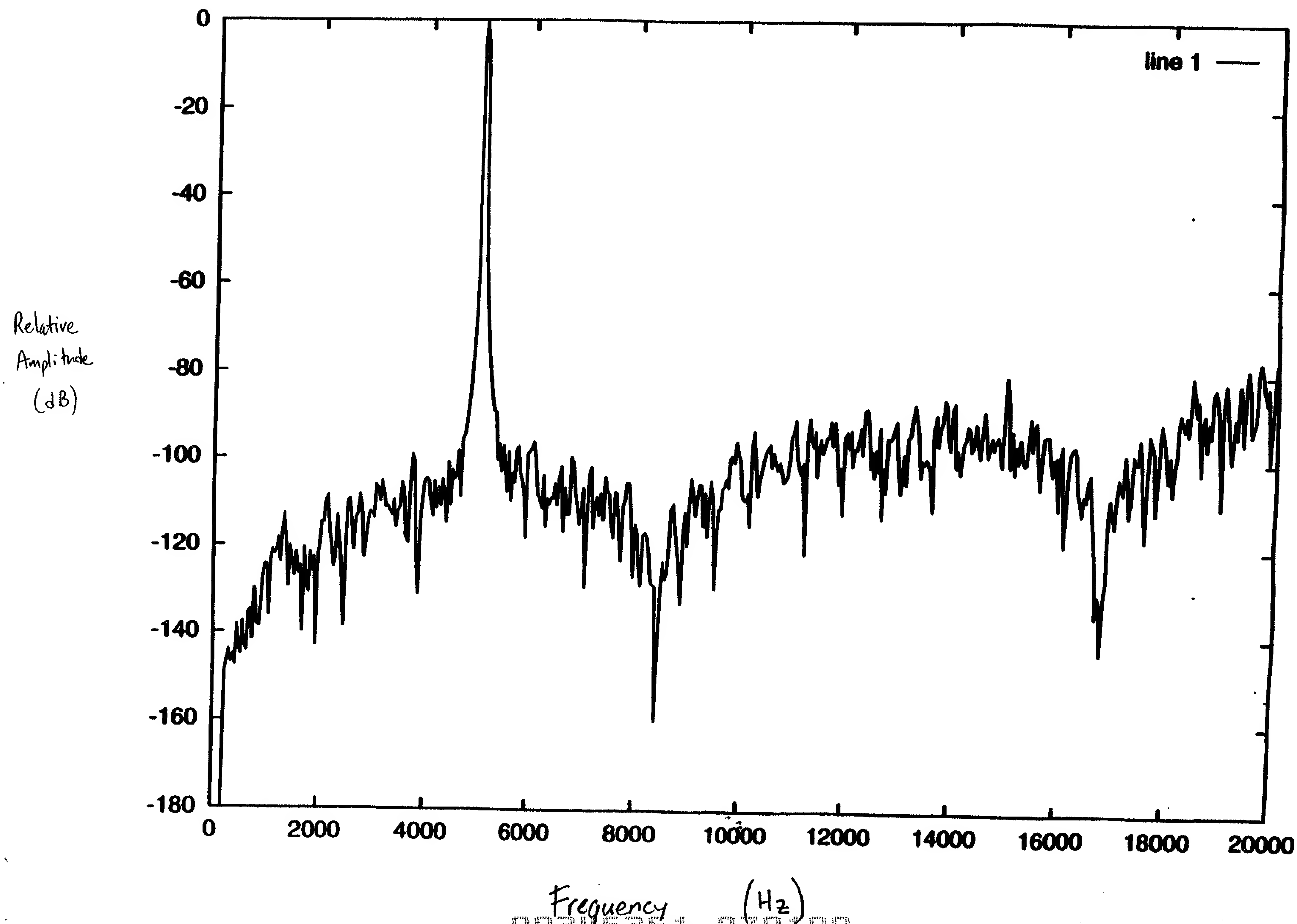

308
402
NOR
430
406
OR
404
AND
440
450
408
AND
310
COMPARATOR OUTPUT
214
410
D Q
412
D Q
D Q
CLOCK
312
314
N FLIP FLOPS

FIG. 5



INPUT 210
α_1
502
504
506
508
510
512
520
522
524
526
528
530
104
318
214
550
$-g_1$
552
$-g_2$
$-\alpha_1$
530
$-\alpha_2$
532
$-\alpha_3$
534
$-\alpha_4$
536
$-\alpha_5$
538
$-\alpha_6$
540
500

FIG. 6



Relative Amplitude (dB)
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
0
2000
4000
6000
8000
10000
12000
14000
16000
18000
20000
line 1
Frequency (Hz)

FIG 7

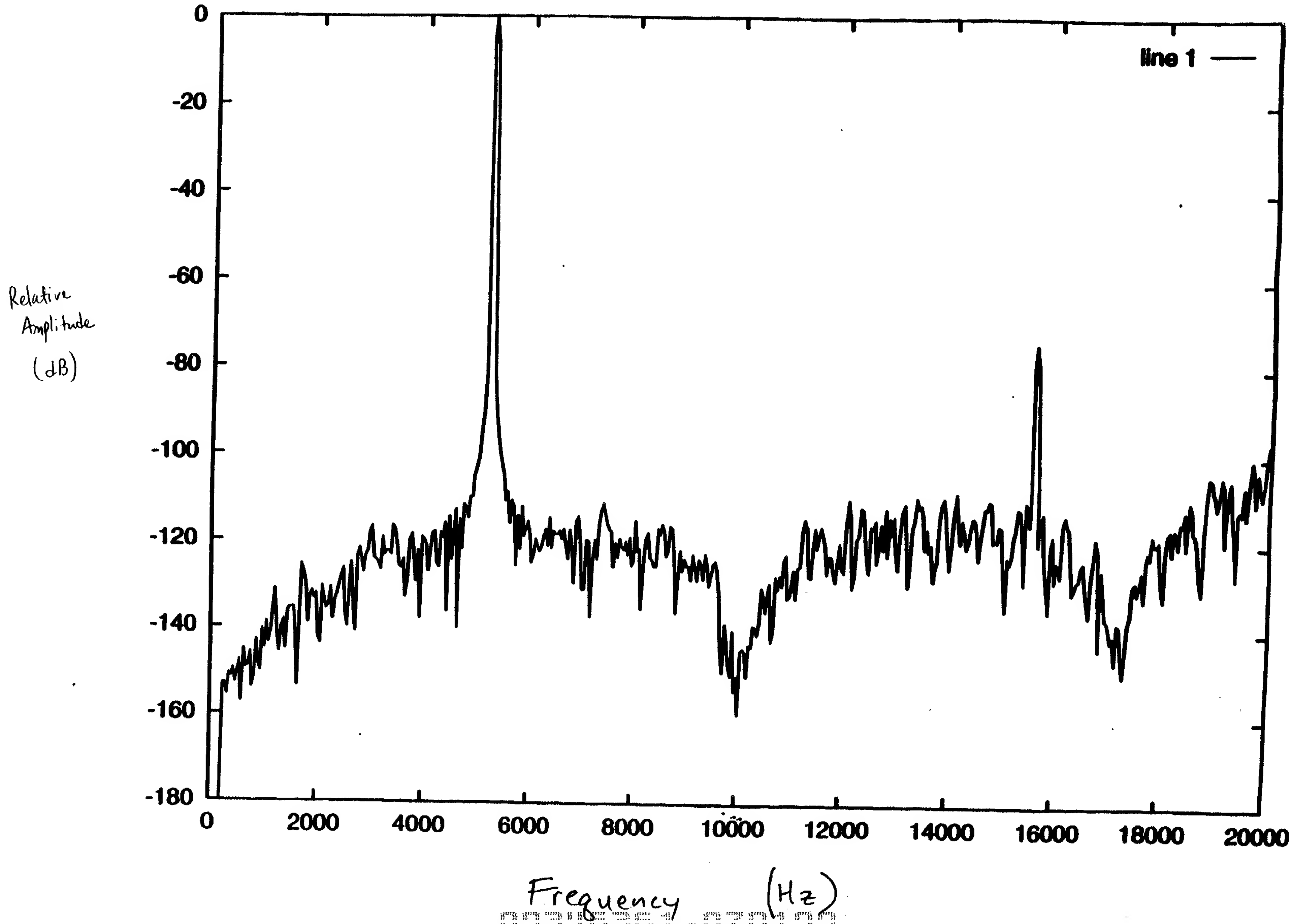
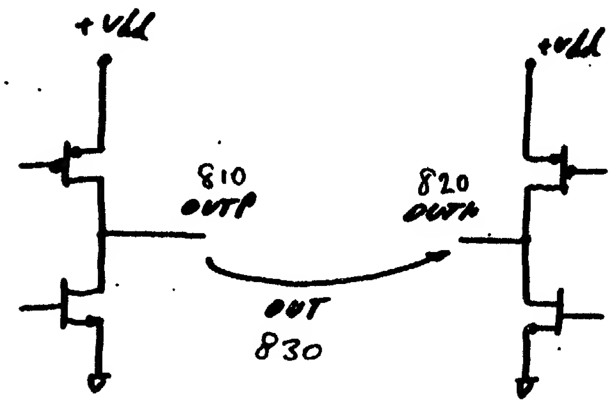

line 1
0
-20
-40
-60
-80
-100
-120
-140
-160
-180
0
2000
4000
6000
8000
10000
12000
14000
16000
18000
20000
Relative Amplitude (dB)
Frequency (Hz)

FIG. 8



(PRIOR ART)

FIG 9

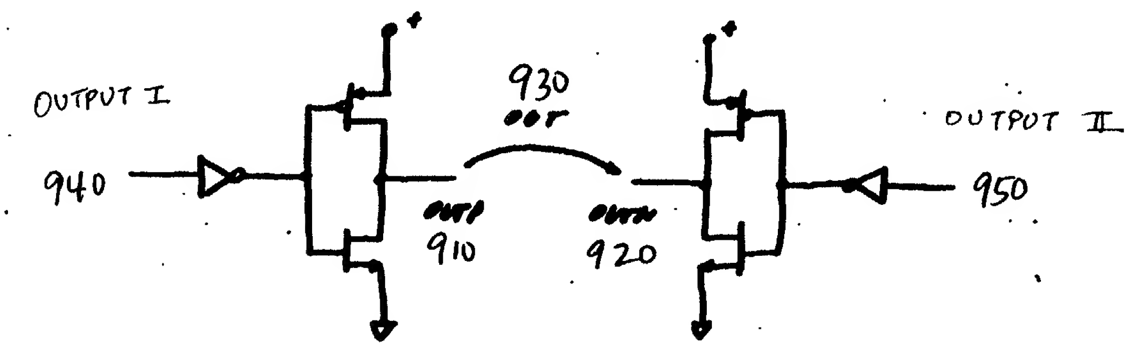
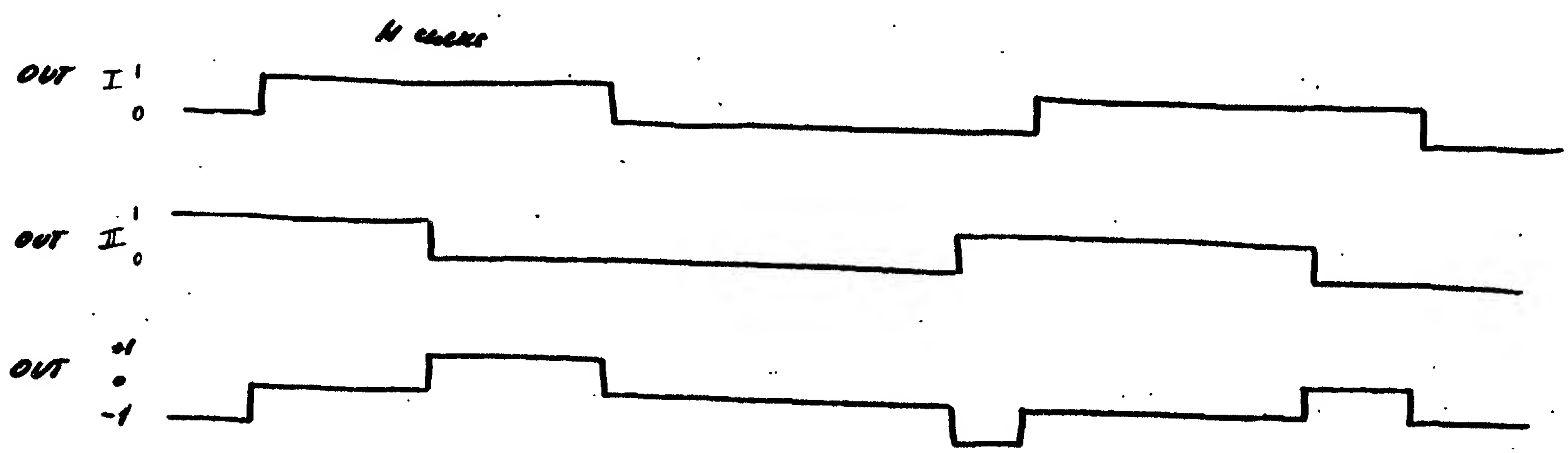


FIG. 10



PATENT
Docket No. 41367-20003.00

COMBINED DECLARATION FOR UTILITY PATENT APPLICATION AND POWER OF ATTORNEY

AS THE BELOW-NAMED INVENTORS, WE HEREBY DECLARE THAT:

Our residences, post office addresss, and citizenships are as stated below next to our names.

We believe we are the original, first and joint inventors of the subject matter which is claimed and for which a patent is sought on the invention entitled: METHOD AND APPARATUS FOR EFFICIENT MIXED SIGNAL PROCESSING IN A DIGITAL AMPLIFIER, the specification of which is attached hereto unless the following box is checked:

☐

WE HEREBY STATE THAT WE HAVE REVIEWED AND UNDERSTAND THE CONTENTS OF THE ABOVE-IDENTIFIED SPECIFICATION, INCLUDING THE CLAIMS, AS AMENDED BY ANY AMENDMENT REFERRED TO ABOVE.

We acknowledge the duty to disclose information which is material to the patentability as defined in 37 C.F.R. § 1.56.

We hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT International application which designated at least one country other than the United States listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed:

Application No.	Country	Date of Filing (day/month/year)	Priority Claimed?
*			☐Yes ☐No

We hereby claim benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below:

Application Serial No.	Filing Date
*	

We hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to

patentability as defined in 37 C.F.R. § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status
*		☐Patented ☐Pending ☐Abandoned

We hereby appoint the following attorneys and agents to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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We hereby declare that all statements made herein of my our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under § 1001 of Title 18 of the United States

Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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